S/N 08/984,560 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jeffrey S. Mailloux et al.	Examiner: Hong C. Kim
Serial No.:	08/984,560	Group Art Unit: 2186
Filed:	December 3, 1997	Docket: 303.623US2
Title:	MEMORY DEVICE WITH PATTERNED AND PATTERNLESS ADDRESSING	

REPLY BRIEF UNDER 37 CFR 1.193(b)

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This Reply Brief is filed in triplicate and presented in response to the Examiner's Answer (the "Answer") dated June 3, 2003. The Appellants respectfully request acknowledgment of receipt, and entry of this Reply Brief in the above-identified Application for review by the United States Patent and Trademark Office Board of Patent Appeals and Interferences (the "Board").

REPLY

Amendments After Final Not Entered

It is noted in the Answer that the amendments in the Appeal Brief filed by the Appellants have not been entered. It is respectfully requested that these amendments to claims 59 and 61, which are suggested by the Appellants solely to provide clarity and consistency in the claim language, and not for reasons related to patentability, be entered.

Grouping of Claims

The Answer asserts that "Applicant has not provided independent argument for each of the claims that allegedly stand alone" and "grouping of claims into ten groups is appropriate." The Appellants respectfully disagree.

In the Appeal Brief filed by the Appellants on April 14, 2003, a specific section (section c.2 found on pgs. 9-13) is devoted to discussion of the separate patentability of each claim. At least one unique feature of each claim is presented, and it is noted for each claim that these features are not disclosed by the cited art. These reasons are bolstered by the detailed argument discussing each of the claims and their relation to the cited art on pages 4-9 of the Appeal Brief.

This type of argument is specifically approved by the M.P.E.P. § 1206, where it is stated that "The appellant must (A) state that the claims do not stand or fall together and (B) present arguments why the claims subject to the same rejection are separately patentable." Further "The reasons may be included in the appropriate portion of the 'Argument' section of the brief." See M.P.E.P. § 1206.

The standard set forth in the M.P.E.P. § 1206 has been met by the Appellants in that the following are provided: (a) a specific statement that the claims do not stand or fall together (see Appeal Brief, pg. 3, part 7), and (b) arguments as to the separate patentability of each claim, both in the form of specific statements (see Appeal Brief, pgs. 9-13, part 8, section c.2), and as a series of arguments (see Appeal Brief, pgs. 4-9, sections c.1.1 and c.1.2). Thus, the Appellants respectfully traverse the assertion in the Answer that "grouping of claims into ten groups is appropriate" and respectfully request consideration of each and every claim independently by the Board.

Compliance with 37 C.F.R. § 1.111(b)

The Answer states that the "Applicant's arguments fail to comply with C.F.R. § 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references." The Appellants respectfully disagree.

In sections c.1.1 and c.1.2 of the Appeal Brief (pgs. 4 and 6), the Appellants set forth specific language which distinguishes the claims from Manning (864), to wit:

(a) Mannning (864) does not disclose "switching circuitry for switching between a first pathway and a second pathway depending on which of said patternless addressing scheme and said patterned addressing scheme is selected" (explicitly claimed by the Appellants in independent claims 11, 62, 65 and 68);

(b) Manning (864) does not disclose "switching circuitry for switching between a first pathway and a second pathway depending on which of said pipeline scheme and said burst scheme is selected" (explicitly claimed by the Appellants in independent claim 59); and

(c) Manning (864) does not disclose "switching circuitry for switching between a ... burst ... pathway and a ... pipeline ... pathway" (explicitly claimed by the Appellants in independent claims 60-61 and 70-71).

To avoid repetitious duplication, it will simply be noted here that Manning (864) fails to disclose many other specific elements with respect to several individual claims, which are delineated on pgs. 5-6 of the Appeal Brief. An explanation as to precisely why such failure attends to the use of Manning begins on pg. 6 of the Appeal Brief, section c.1.2 (i.e., "Why the reference does not disclose the claimed subject matter in as complete detail as is contained in the claim."). Therefore, the Appellants respectfully traverse the assertion in the Answer that the "Applicant's arguments fail to comply with C.F.R. § 1.111(b)" and request withdrawal of this statement.

Response by Appellants to General Arguments in the Answer

The statements in the Answer that "Manning (864) discloses switching circuitry for switching between a first pathway and a second pathway ... depending on which of a patternless addressing scheme ... and a patterned addressing scheme ... is selected" does not distinguish between the operation of a pipeline architecture (which may include a pipeline stage) and a pipeline mode, as described in detail by the Appellants (see Appeal Brief, pgs. 11-12). Similarly, the assertions in the Answer that "Manning discloses ... switching between fast page mode, EDO page mode, static column mode and burst operation" does not take into account the following points made by the Appellants:

(a) Manning (864) does not disclose selecting or switching between pipelined and burst modes; and

(b) the Office has admitted that "Manning [864] does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." in an Office Action mailed to the Appellants on July 18, 2001 (Application Ser. No. 08/984,701, Paper 19, page 7) with regard to similar subject matter.

The statement is made in the Answer that "... in order to work in a standard EDO memory including a pipelined architecture, one has to select a pipelined mode if one is in a burst mode." This statement mischaracterizes the operation of an EDO memory (e.g., an EDO

memory with internal addresses generated using a pipeline stage/architecture does not require selecting a "pipelined mode" for operation by receiving *external addresses*, as defined by the Appellants). Further, there is no evidence in the record of this specific type of construction or operation in Manning (864).

Several other statements of alleged fact, unsupported by any reference, are presented in the Answer. While the Appellants have repeatedly requested evidentiary support for similar statements, none has been given. A few of these statements are quoted below:

(a) "it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input, or memory data output to be processed simultaneously";

(b) "the pipelined architecture requires only a single sample-and-hold circuit per read or write circuit"; and

(c) "pipelined architecture can be used on standard EDO, fast page mode, static column, and burst modes (see col. 7 lines 50-54)".

However, other than these unsupported statements, there is no evidence whatsoever that Manning (864) teaches this specific type of operation or construction. The text of Col. 7, lines 50-54 merely states "A more complex memory device may provide additional modes ... such as switching between fast page mode, EDO page mode, static column mode and burst operation through the use of various combinations of /WE and /OE at /RAS falling time." This is obviously not a reference to a pipelined mode of operation. Further, as explained in the Appeal Brief (see Appeal Brief pgs. 11-12), and in the reference cited by the Appeal Brief (see Appeal Brief, Appendix II), none of these modes necessarily have anything to do with a true pipelined mode of operation. Thus, the assertion that Manning (864) teaches a pipelined mode of operation is simply not supported by the evidence in the record.

Finally, it is respectfully noted that a Notice of Allowability (the "Notice") indicating allowance of all claims was mailed to the Appellants (Paper 32) in U.S. Patent Application Serial Number 08/984,561; Atty. Ref:303.623US6, the appeal of which is no longer before the Board. The Office has admitted the deficiencies of Manning (864) in this related matter with respect to several elements claimed by the Appellants in the instant Application. The attention of the

Board is directed to the following assertions by the Appellants in the appeal of U.S. Application Serial No. 08/984,561:

> "Manning Col. 6, lines 14-34 merely describe burst and "standard" (i.e., page mode - see col. 6, lines 18-19) EDO operations. Manning Col. 7, lines 43-54 speaks to switching between non-EDO and EDO page modes, a static column mode, and a burst mode. Thus, **Manning never discusses the ability to select or switch between burst and pipelined modes of operation**..." (emphasis added)

This language was approved by the Office in the Notice, which states: "The claims are allowable over the prior art of record [U.S. Patent No. 5,587,964, issued to Rosich et al. in view of Manning (864)] because the claims are distinguished from the prior art of record for the reasons as set forth in the ... appeal filed on 12/27/02 and because an update of a search previously made does not detect the combined claimed elements as set forth in claims 1-23." For example, claim 72 of U.S. Application Serial No: 08/984,561 reads:

> A method for switching between pipeline and burst modes of operation, comprising:
> maintaining a first enabling signal in an active state, the first enabling signal being an address-strobe signal;
> maintaining an external mode select signal to select a pipeline mode;
> receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses; and
> switching the mode of operation to a burst mode on successive cycles of the second enabling signal while maintaining the first enabling signal in the active state.

Thus, the Office agrees that Manning (864) does not teach the ability to select or switch between burst and pipelined modes of operation, and the standard of § 102 has not been met, since "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131.

Response by the Appellants to Specific Arguments in the Answer

Specific references to claims in the Answer are separated into ten groups. To simplify coordinating the responses to these arguments, the Appellants will reply in accordance with the grouping. However, this response format is in no way to be construed as an admission that such grouping is appropriate, as alleged in the Answer. The response for each group will be presented in the form of a statement in the Answer, and a factual correction in the response.

Group I:

Statement -- Manning discloses ... circuitry for switching between a first/pipelined pathway and a second/burst pathway .... .

Response – There is no evidence in the record that Manning (864) discloses any kind of circuitry to switch to/from a pipelined mode of operation as defined by the Appellants in the Application. As noted above, the Office has already admitted that "Manning [864] does not specifically disclose a mode select pin and a mode control signal for selecting between a burst and a pipeline mode of operation." with respect to Application Ser. No. 08/984,701, Paper 19, page 7. Further, as noted above, the Office has agreed with the Appellants in the appeal of U.S. Application Serial No: 08/984,561 that Manning (864) does not disclose any way to switch between pipelined and burst modes.

Group II:

Statement – Manning (864) discloses a temporary buffer for providing an external address.

Response -- The mere existence of a latch/counter (called "buffer" in the Answer) in Manning (864), without more, is insufficient to satisfy the requirements of § 102, since "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Id.* There is no evidence in the record that the latch/counter of Manning (864) operates as claimed by the Appellants in claims 13 and 62-63 (e.g., wherein the internal address [generated by the counter] is provided to the temporary storage device *through the switching circuitry*).

Group III:

Statement – Manning (864) discloses a multiplexed device ... during the burst mode, an internal counter/latch path is selected, however, during the pipelined mode, an external counter/latch path is selected.

Response – First, the element designated as a "multiplexed device" (Fig. 1, Ref. 26) in the Answer is a counter/latch, not a multiplexer. Second, even if this element did operate as a multiplexed device, the mere existence of a multiplexer in Manning (864), without more, is insufficient to satisfy the requirements of § 102, since "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Id.* Finally, this detailed description in the Answer reads a functionality into Manning (864) which simply does not exist. The cited text (col. 6, lines 26-34) speaks of controlling the counter/latch in conjunction with burst, non-burst, interleaved, and linear addressing modes– which have nothing to do with a pipelined mode of operation. Finally, this interpretation of elements by the Answer (see argument in Group II above) forces the counter and the multiplexed device claimed by the Appellants to be the same element, which is not what is claimed (see claims 15 and 19 of the Application).

Group IV:

Statement – Manning (864) discloses random column access as part of the pipelined architecture ... since a new (random) address is provided to an address input terminal every cycle during a pipelined mode of operation. ... a new external address should be provided to an input address terminal every memory access cycle ...

Response – The assertion in this case is unsupported by any evidence in the record. Nothing in Manning (864) describes this specific method of operation, as admitted in the Answer (which resorts to the use of the word "should" when describing this type of operation, rather than a specific reference to the text of Manning).

Group V:

Statement – Manning (864) discloses pipelined and burst EDO patterns.

Response – As admitted in the fourth paragraph of the Answer, pg. 11, "Manning (864) discloses ... switching between burst EDO mode and standard EDO mode". Asserting that the pipelined mode is necessarily the same as an EDO mode clearly contradicts the reference

supplied by the Appellants in Appendix II of the Appeal Brief, and is not supported by the text of Manning (864), nor by the text of the Answer itself.

Group VI:

Statement – Manning (864) discloses an asynchronous device.

Response – The mere use of the term "asynchronous" in conjunction with memory in Manning (864), without more, is insufficient to satisfy the requirements of § 102, since "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Id.* There is no evidence in the record that the memory described by Manning (864) is able to switch "between a first pathway and a second pathway depending on which of said patternless ... and said patterned addressing scheme is selected" as claimed by the Appellants. Again, as noted above, the Office has agreed with the Appellants in the appeal of U.S. Application Serial No: 08/984,561 that Manning (864) does not disclose any way to switch between pipelined and burst modes.

Group VII:

Statement – Manning (864) discloses a decoder.

Response – The mere existence of a decoder in Manning (864), without more, is insufficient to satisfy the requirements of § 102, since "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Id.* There is no evidence in the record that the decoder of Manning (864) is for switching "between a first pathway and a second pathway depending on which of said patternless ... and said patterned addressing scheme is selected" as claimed by the Appellants.

Group VIII:

Statement – Manning discloses a counter.

Response – The mere existence of a counter in Manning (864), without more, is insufficient to satisfy the requirements of § 102, since "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Id.* There is no evidence in the record that the counter of Manning (864) is for switching "between a first pathway and a second pathway

depending on which of said patternless ... and said patterned addressing scheme is selected" as claimed by the Appellants.

Group IX:

Statement – Manning (864) discloses [sic] internal address is provided to the temporary device through the switching circuit.

Response – It is unclear what is meant by "temporary device" here. Assuming it is a storage device, the cited text (col. 3 lines 20-23 and Fig. 1) merely refers to incrementing addresses via internal burst operations. Nothing in the text or figure speaks to providing an internal address "through the switching circuitry" as claimed by the Appellants.

Group X:

Statement – Manning (864) discloses an interleaved address access and a liner [sic] address access.

Response – The mere use of the terms "interleaved" and/or "linear" in conjunction with memory access in Manning (864), without more, is insufficient to satisfy the requirements of § 102, since "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Id.* There is no evidence in the record that the memory described by Manning (864) is able to switch "between a first pathway and a second pathway depending on which of said patternless ... and said patterned addressing scheme is selected" as claimed by the Appellants. Again, as noted above, the Office has agreed with the Appellants in the appeal of U.S. Application Serial No: 08/984,561 that Manning (864) does not disclose any way to switch between pipelined and burst modes.

CONCLUSION

For these reasons, it is respectfully submitted that a *prima facie* case of anticipation under 35 U.S.C. §102 has not been established. Therefore, it is respectfully requested that the rejection of claims 11-21 and 59-71 be reconsidered and withdrawn. The Examiner is invited to telephone Appellants' attorney, Mark Muller, at (210) 308-5677, or the undersigned to facilitate prosecution of this Application. Should the Board be of the opinion that any rejected claim is allowable in amended form, an explicit statement to that effect is also respectfully requested. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,
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